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HARNESS, DICKEY & PIERCE P.L.C.			PATEL, HETUL B	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/627,269	CHEN ET AL.
	Examiner	Art Unit
	Hetul Patel	2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 16 May 2007.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-4,6-17,19-53,55,57-62 and 64-74 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-4,6-17,19-53,55,57-62 and 64-74 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This Office Action is in response to the claim amendment and remarks filed on May 16, 2007. This amendment has been entered and carefully considered. Claim 75 is cancelled; and none of the claims are newly added. Therefore, claims 1-4, 6-17, 19-53, 55, 57-62 and 64-74 are currently pending in this application.
2. Applicant's arguments with respect to claim 1 and other independent claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 8-17, 21-26, 49-53, 55, 57-62 and 64-74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaggar (USPN: 5,701,493) in view of Shelor (USPN: 7,024,544).

As per claim 1, Jaggar teaches a register system for a data processing system comprising an unbanked memory unit (i.e. the stack memory area) having a plurality of registers (i.e. memory locations) addressable by an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8), wherein the encoded address corresponds to a respective one of the plurality of registers (i.e.

registers R0-R13 in Figs. 1 and 8) and a corresponding processor mode (i.e. a user mode and system mode); input ports (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8) to receive inputs for addressing at least one register using an encoded address; and output ports (i.e. the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8) to output data from at least one register addressable by an encoded address (e.g. see the abstract and Figs. 1 and 8). Jaggar further teaches an (common) address encoder (i.e. the combination of components 12-20 in Fig. 8) for all input ports, the address encoder to provide an encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) for accessing one of the plurality of registers (i.e. R0-R15 in Fig. 8) (e.g. see Fig. 8).

However, Jaggar does not teach about having a plurality of encoders, a respective one of them for each of the input ports as claimed. Shelor, on the other hand, teaches about having an address encoder (i.e. 280 in Fig. 3) for providing encoded address for accessing one of the memory locations (e.g. see Col. 6, lines 16-21 and Fig. 3). Shelor further discloses that a separate address encoder for each of the input ports (i.e. signal lines) may be provided (e.g. see Col. 6, lines 39-41). Accordingly, it would have been obvious to one of ordinary skills in the art at the time of the current invention was made to have a separate address encoder for each of the input port in the register system of Jaggar as taught by Shelor. In doing so, it increases the overall performance of the data processing system by providing the encoded addresses for all inputs in parallel compared to one by one. Therefore, it is being advantageous. Shelor further teaches that each of the plurality of registers has an address having a length of x

bits (i.e. 4 bits as shown in Fig. 3, element 213), each of the processor modes has a length of y bits (i.e. 5 bits as shown in Fig. 3, element 215), and the encoded address has a length (i.e. 5 bits as shown in Fig. 3, element 216) that is less than $x + y$ bits (i.e. less than $4+5=9$ bits) (e.g. see Fig. 3).

As per claim 2, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches that the encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8) identifies a general purpose register (i.e. registers R0-R13 in Figs. 1 and 8) associated with a processor mode (i.e. a user mode and system mode) (e.g. see the abstract and Figs. 1 and 8).

As per claim 3, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches that each register (i.e. R0-R15 in Fig. 8) is associated with a register index (i.e. 0000-1111, 17 in Fig. 8) that maps to an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8) based on at least one processor mode (i.e. a user mode and system mode) (e.g. see Figs. 1 and 8).

As per claim 4, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches that the input ports (i.e. the "reg add", mode bits input to 17 and input to 8 in Fig. 8) receive at least one source register index input (i.e. the register address input) and processor mode input (i.e. the mode bits input) for use in providing an encoded address (i.e. the combination of

register address and the mode bits, 17 in Fig. 8) for accessing at least one register (i.e. R0-R15 in Fig. 8) (e.g. see Fig. 8).

As per claim 8, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches that data for one or more instructions being processed is outputted from the unbanked memory unit (i.e. the MMU 62 in Fig. 8) (e.g. see Fig. 8).

As per claim 9, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches that the register system further comprising input ports (i.e. the "reg add", mode bits input to 17 and input to 8 in Fig. 8) to receive at least one write index input (i.e. the register address input) and processor mode input (i.e. the mode bits input) for use in providing the encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) for writing data to at least one register (i.e. to R0-R15 in Fig. 8); and at least one write input port (i.e. input port to the read buffer 8 shown in Fig. 8) for writing the data to the register (i.e. R0-R15 in Fig. 8) addressable by the encoded address (e.g. see Fig. 8).

As per claim 10, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches that data for one or more executed instructions (i.e. instructions/commands buffered in instruction register 12 in Fig. 8) for the data processing are written into the unbanked memory unit (i.e. MMU 62 in Fig. 8) (e.g. see Fig. 8).

As per claim 11, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches that the processor mode includes exception handling modes (i.e. a plurality of IRQ32 etc.) (e.g. see the abstract).

As per claim 12, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches that the exception handling processor modes include the interrupt request (IRQ) mode (i.e. IRQ32), the fast interrupt request (FRQ) mode (i.e. FRQ32), the undefined instruction (UND) mode (i.e. Undef32) and the abort exception (ABT) mode (i.e. Abt32) (e.g. see the abstract and Col. 2, lines 45-58).

As per claims 14-17 and 21-25, see arguments with respect to the rejection of claims 1-4 and 8-12, respectively. Claims 14-17 and 21-25 are also rejected based on the same rationale as the rejection of claims 1-4 and 8-12, respectively.

As per claims 13 and 26, Jaggar teaches the claimed invention as described above and furthermore, Jaggar teaches that each exception handling mode corresponds to one or more registers (e.g. see Col. 2, lines 45-58).

As per claim 49, the combination of Jaggar and Shelor teaches a microprocessor comprising an integrated circuit comprising a unbanked memory unit (i.e. the stack memory area) having a plurality of registers (i.e. memory locations) addressable by an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8), wherein the encoded address corresponds to a respective one of the plurality of registers (i.e. registers R0-R13 in Figs. 1 and 8) and a corresponding processor mode (i.e. a user mode and system mode); and at least one address encoder (i.e. the

combination of components 12-20 in Fig. 8) to provide at least one encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) for addressing at least one of the plurality of registers (i.e. R0-R15 in Fig. 8); a plurality of inputs (i.e. the reg address from 14 and the mode bits from 18 as shown in Fig. 8) to receive index (i.e. reg address 17 shown in Fig. 8) and processor mode information (i.e. the mode bits 17 shown in Fig. 8) for use in providing the encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8), at least one output to output data stored in the storage location addressable by the encoded address (e.g. see the abstract and Figs. 1 and 8). Jaggar further teaches an address encoder (i.e. the combination of components 12-20 in Fig. 8) for each input port, the address encoder to provide an encoded address (i.e. the combination of register address and the mode bits, 17 in Fig. 8) for accessing one of the plurality of registers (i.e. R0-R15 in Fig. 8) (e.g. see Fig. 8). Examiner interpreting the limitation "an address encoder for each input port" as the *same* address encoder for each input port.

As per claims 50-53 and 55, see arguments with respect to the rejection of claims 2-3, 11-12 and 9, respectively. Claims 50-53 and 55 are also rejected based on the same rationale as the rejection of claims 2-3, 11-12 and 9, respectively.

As per claim 57, see arguments with respect to the rejection of claim 49. Claim 57 is also rejected based on the same rationale as the rejection of claim 49.

As per claims 58-62 and 64, see arguments with respect to the rejection of claims 2-3, 11-12 and 9, respectively. Claims 58-62 and 64 are also rejected based on the same rationale as the rejection of claims 2-3, 11-12 and 9, respectively.

As per claim 65, the combination of Jaggar and Shelor teaches an integrated circuit method comprising configuring the integrated circuit to receive processor mode (i.e. a user mode and system mode) and source data inputs (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8); configuring the integrated circuit to determine an encoded address based on the processor mode and source data inputs, wherein the encoded address corresponds to a respective one of a plurality of registers (i.e. memory locations) and a corresponding processor mode (i.e. a user mode and system mode); configuring the integrated circuit to address one of the registers using an encoded address; and configuring the integrated circuit to output data from the register addressable by the encoded address (i.e. the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8) (e.g. see the abstract and Figs. 1 and 8).

As per claim 66, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches about configuring the integrated circuit to output data for multiple instructions (i.e. via the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8).

As per claim 67, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches about configuring the integrated circuit to write data to one of the registers addressable by an encoded address (e.g. see the abstract).

As per claim 68, the combination of Jaggar and Shelor teaches the claimed invention as described above and furthermore, Jaggar teaches about configuring the integrated circuit to write data to one of the registers for multiple executed instructions

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(i.e. via the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8).

As per claims 69-74, see arguments with respect to the rejection of claims 1, 65, 65 and 66-68, respectively. Claims 69-74 are also rejected based on the same rationale as the rejection of claims 1, 65, 65 and 66-68, respectively.

4. Claims 6-7 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaggar in view of Shelor, further in view of Meier et al. (USPN: 6,363,471) hereinafter, Meier.

As per claims 6 and 7, the combination of Jaggar and Shelor teaches the claimed invention as described above, but failed to teach a latch circuit and a selector as claimed. Meier, however, teaches about using the latch or other clocked storage devices to store the intermediate values for pipelining to the next stage (e.g. see Col. 16, lines 21-35 and Fig. 6). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement Meier's latch circuit in the register system taught by the combination of Jaggar and Shelor. In doing so, this latch circuit can buffer the data (i.e. the encoded addresses) for pipeline storage in case if the data can be reused. The further limitation of having the selector coupled to the latch and the address encoder is well-known and notorious old in the art at the time of the current invention was made. By using the selector, such as a mux, the encoded address can be selected either from the latch circuit or directly from the

address encoder based on a select signal. The Examiner herein taking Official Notice on this subject matter.

As per claims 19-20, see arguments with respect to the rejection of claims 6-7, respectively. Claims 19-20 are also rejected based on the same rationale as the rejection of claims 6-7, respectively.

5. Claims 27-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaggar in view of Kerr et al. (USPN: 2003/0159021) hereinafter, Kerr.

As per claim 27, the combination of Jaggar and Shelor teaches a data processing system comprising a microprocessor (i.e. 62 in Fig. 8) comprising a register system, the register system including a unbanked memory unit (i.e. the stack memory area) having a plurality of registers (i.e. memory locations) addressable by an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8), wherein the encoded address corresponds to a respective one of the plurality of registers (i.e. registers R0-R13 in Figs. 1 and 8) and a corresponding processor mode (i.e. a user mode and system mode); input ports (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8) to receive inputs for addressing at least one register using an encoded address; and output ports (i.e. the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8) to output data from at least one register addressable by an encoded address (e.g. see the abstract and Figs. 1 and 8). Jaggar further teaches an address encoder (i.e. the combination of components 12-20 in Fig. 8) for each input port, the address encoder to provide an encoded address

(i.e. the combination of register address and the mode bits, 17 in Fig. 8) for accessing one of the plurality of registers (i.e. R0-R15 in Fig. 8) (e.g. see Fig. 8). Examiner interpreting the limitation "an address encoder for each input port" as the same address encoder for each input port.

However, both Jaggar and Shelor failed to teach that the microprocessor comprising a plurality of pipeline stages. Kerr, on the other hand, teaches the microprocessor (i.e. the TMC core, 600 in Fig. 6) comprising a plurality of pipeline stages (i.e. 610, 620, 630 and 660 in Fig. 6) (e.g. see paragraph [0003] and Fig. 6). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the plurality of pipeline stages taught by Kerr in the data processing system of the combination of Jaggar and Shelor. In doing so, a number of instructions are being executed in parallel and as a result of that the overall performance of the data processing system increases.

As per claim 28, the combination of Jaggar, Shelor and Kerr teaches the claimed invention as described above and furthermore, Jaggar teaches that the encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8) identifies a general purpose register (i.e. registers R0-R13 in Figs. 1 and 8) associated with a processor mode (i.e. a user mode and system mode) (e.g. see the abstract and Figs. 1 and 8).

As per claims 29, 31 and 32, the combination of Jaggar, Shelor and Kerr teaches the claimed invention as described above and furthermore, Kerr teaches that the pipeline stages include an instruction fetch stage (i.e. IF 610 in Fig. 6) to fetch one or

more instructions; an instruction decode stage (i.e. ID 620 in Fig. 6) to decode fetched instructions from the instruction fetch stage, the instruction decode stage to forward inputs to the memory unit (i.e. 640 in Fig. 6) for outputting data from or writing data to one or more of the registers (i.e. 652, 654 in Fig. 6), an execution stage (i.e. EX 630 in Fig. 6) including a plurality of execution units (i.e. 646 and 656 in Fig. 6), each execution unit to receive data from the register system for executing an instruction, and a write back or retire logic stage (i.e. WB 660 in Fig. 6) to receive results data associated with one or more instructions executed by the execution units of the execution stage, and to forward the results data to the register system for storage (i.e. via bus 426 in Fig. 6) (e.g. see Fig. 6 and paragraphs [0038]-[0040]).

As per claim 30, the combination of Jaggar, Shelor and Kerr teaches the claimed invention as described above and furthermore, Jaggar teaches that the register system further includes a plurality of input ports (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8) to receive inputs from the instruction decode stage, the inputs being used to obtain the encoded address for accessing at least one register; and at least one output port (i.e. the output to write buffer 10 and the output to the internal bus 4 in Figs. 1 and 8) to output data from the register addressable by the encoded address (e.g. see Figs. 1 and 8).

As per claim 33 the combination of Jaggar, Shelor and Kerr teaches the claimed invention as described above and furthermore, Jaggar teaches that the register system further includes a plurality of input ports (i.e. the input from the read buffer 8 and the input from the internal bus 4 in Figs. 1 and 8) to receive the data from the write back or

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retire logic for one or more executed instructions, the data to be written in the register system (e.g. see Figs. 1 and 8).

As per claim 34, the combination of Jaggar, Shelor and Kerr teaches the claimed invention as described above and furthermore, Jaggar teaches that each register (i.e. R0-R15 in Fig. 8) is associated with a register index (i.e. 0000-1111, 17 in Fig. 8) that maps to an encoded address (i.e. the combination of register address and the mode bits, 17 in Figs. 1 and 8) based on at least one processor mode (i.e. a user mode and system mode) (e.g. see Figs. 1 and 8).

As per claim 35, the combination of Jaggar, Shelor and Kerr teaches the claimed invention as described above and furthermore, Jaggar teaches that the processor mode includes exception handling modes (i.e. a plurality of IRQ32 etc.) (e.g. see the abstract).

As per claim 36, the combination of Jaggar, Shelor and Kerr teaches the claimed invention as described above and furthermore, Jaggar teaches that the exception handling processor modes include the interrupt request (IRQ) mode (i.e. IRQ32), the fast interrupt request (FRQ) mode (i.e. FRQ32), the undefined instruction (UND) mode (i.e. Undef32) and the abort exception (ABT) mode (i.e. Abt32) (e.g. see the abstract and Col. 2, lines 45-58).

As per claim 37, the combination of Jaggar, Shelor and Kerr teaches the claimed invention as described above and furthermore, Jaggar teaches that each exception handling mode corresponds to one or more registers (e.g. see Col. 2, lines 45-58).

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As per claims 38-48, see arguments with respect to the rejection of claims 27-37, respectively. Claims 38-48 are also rejected based on the same rationale as the rejection of claims 27-37, respectively.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on 8:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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